IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method, comprising:

recording an address of a write operation to a memory having information cached by a non-volatile cache prior to executing an operating system cache driver associated with the non-volatile cache;

recording the address of the write operation in a log;

setting a flag to indicate an overrun of the log; and

invalidating the information if the flag is set.

2. (Canceled)

3. (Currently Amended) The method of claim 1 [[2]], wherein the log is stored in a memory comprising at least one of a static random access memory (SRAM), a dynamic random access memory (DRAM), a flash memory, and a polymer ferroelectric RAM (PFRAM).

4. (Original) The method of claim 1, further comprising:

detecting the write operation.

5. (Original) The method of claim 4, wherein detecting the write operation further comprises:

trapping an interrupt request.

6. (Original) The method of claim 1, further comprising:

modifying data corresponding to the address of the write operation.

7. (Original) The method of claim 6, wherein modifying the data corresponding to the address of the write operation further comprises:

updating the data corresponding to the address of the write operation.

8. (Original) The method of claim 6, wherein modifying the data corresponding to the address of the write operation further comprises:

invalidating the data corresponding to the address of the write operation.

9. (Currently Amended) An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

recording an address of a write operation to a memory having information cached by a non-volatile cache prior to executing an operating system cache driver associated with the non-volatile cache;

recording the address of the write operation in a log;

setting a flag to indicate an overrun of the log; and

invalidating the information if the flag is set.

10. (Canceled)

11. (Currently Amended) The article of claim 9 [[10]], wherein the log is included in a non-volatile memory.

12-13. (Canceled)

14. (Currently Amended) An apparatus, comprising:

a non-volatile cache; [[and]]

a first memory to store an address associated with a write operation to a second memory having information cached by the non-volatile cache prior to executing an operating system cache driver associated with the non-volatile cache;

the first memory to record the address of the write operation in a log; and

a machine to set a flag to indicate an overrun of the log; and

the machine to invalidate the information if the flag is set.

15. (Original) The apparatus of claim 14, wherein the address is a logical block address.

16. (Currently Amended) The apparatus of claim 14, wherein the first memory to store an address comprises a non-volatile memory.

17. (Original) The apparatus of claim 14, further comprising:

a module to receive an interrupt request associated with the write operation.

18. (Original) The apparatus of claim 17, wherein the interrupt request is a basic input-output system Int13h request.

19. (Currently Amended) A system, comprising:

a non-volatile cache; [[and]]

a first memory to store an address associated with a write operation to a second memory having information cached by the non-volatile cache prior to executing an operating system cache driver associated with the non-volatile cache;

a processor coupled to the first memory to store an address;

the first memory to record the address of the write operation in a log;

the processor to set a flag to indicate an overrun of the log;

the processor to invalidate the information if the flag is set; and

a display coupled to the processor.

20. (Original) The system of claim 19, further comprising:

a module to receive an interrupt request associated with the write operation.

21. (Original) The system of claim 20, wherein the module is included in a device option memory.

22. (Original) The system of claim 20, wherein the module is included in a basic input-output system.

23. (Currently Amended) The system of claim 19, wherein the first memory to store an address comprises a non-volatile memory to store the [[a]] log including a plurality of memory addresses including the address of the write operation.